AMENDMENTS TO THE SPECIFICATION

In the original specification on page 9, lines 20-28, please amend the paragraph in the specification as follows:

Hence, control of a dual expander can be accomplished to both ~~and~~ write and read data to and from internal registers in either of the expander cores using a single test port, such as a J-tag port. Access to, and control of, each of the expander cores in the dual expander is accomplished by placing one of the expander cores in bypass mode. Since the expander core in bypass mode functions as a one-bit serial shift register, dummy bytes must be provided to ensure correct data is provided to the internal shift registers of the expander cores. The necessity for removing and reprogramming EPROMs has been eliminated and the host 100 can provide complete control of each expander core in a dual expander in a simple and easy fashion.